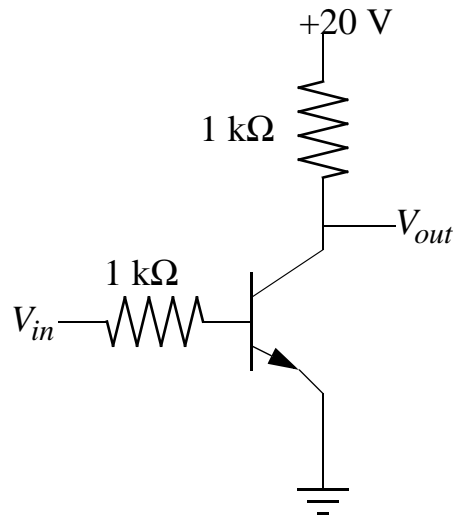


# *Pulse Measurement*



# Transistor Switch

- Bipolar Junction Transistor (BJT) in common emitter mode



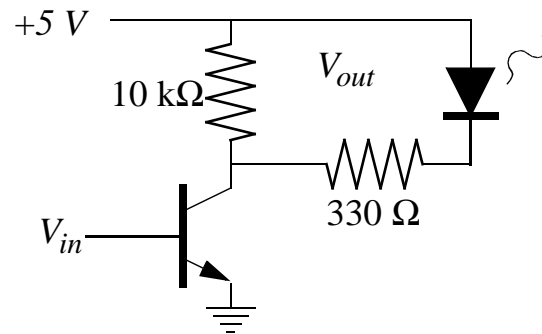
- When  $V_{in} = 0\text{ V}$  the transistor switch is open (off) and  $V_{out} = 20\text{ V}$ .
- As  $V_{in}$  increases above  $0.6\text{ V}$  then transistor turn on and current begins to flow, lowering  $V_{out}$  towards ground.
- The base of the transistor will hold at  $0.7\text{ V}$  and when  $V_{in} = 0.9\text{ V}$ ,  $I_B = 0.2\text{ mA}$  and  $I_C = \beta I_B = 20\text{ mA}$ . The voltage drop to the collector would now be  $20\text{ V}$  and the transistor will be fully on and  $V_{out} = 0.2\text{ V}$ .
- With the exception of the range from  $0.6\text{ V} < V_{in} < 0.8\text{ V}$ , this circuit has only two output states.

# Indicator Light

- Current should be either on or off. Typically a transistor switch, logic gate, or saturated op-amp will drive the LED.
- Use  $V_{CC} = +5\text{ V}$ ,  $V_{LED} = 1.7\text{ V}$ ,  $I_{LED} = 10\text{ mA}$ .

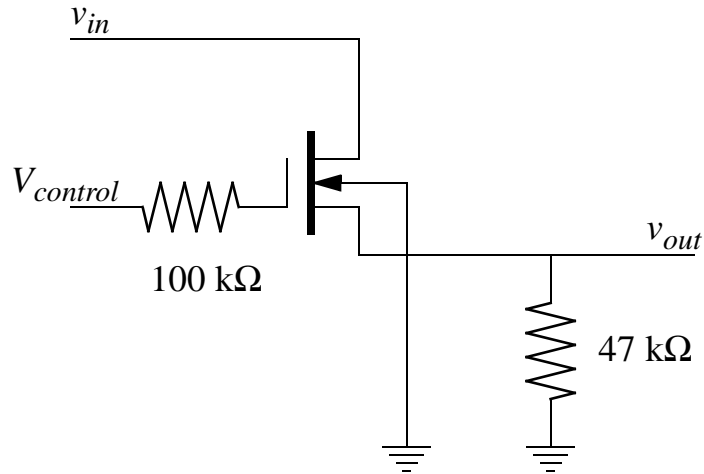
$$R = \frac{V_{CC} - V_{LED}}{I_{LED}} = 330\Omega$$

- Driving circuit ( $V_{in} > 0$ , LED is on)



# MOSFET Switch

- Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is controlled either ON or OFF



There is a voltage divider with  $R_{DS}$  and the  $47\text{ k}\Omega$  resistor.

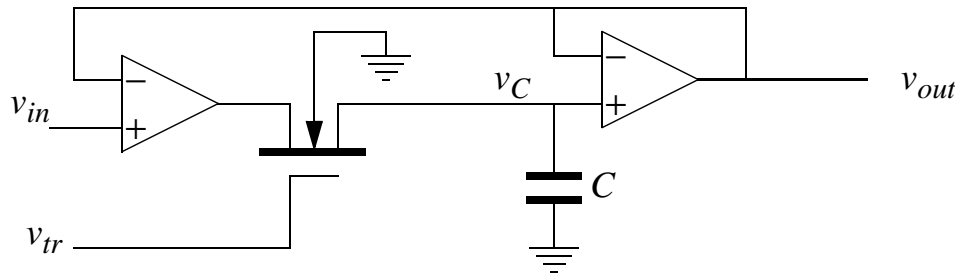
When the gate is ground or negative,  $R_{DS} > 10^{10}\ \Omega$ ,  $v_{out} < 0.0001v_{in}$ .

When the gate is  $+15\text{ V}$ ,  $R_{DS} = 100\ \Omega$ ,  $v_{out} = 0.998 v_{in}$ .

- The MOSFET switch is bidirectional, like a mechanical switch  
The gate is not fully functional if the signal is near  $V_{control}$ .

# Sample and Hold

- Two x1 buffers can be combined with a MOSFET switch to create a circuit that selects voltages at specific times.



When  $v_{tr} = -15$  V, the MOSFET is non-conducting and  $v_{out} = v_C$ .

When  $v_{tr} = +15$  V, the MOSFET is conducting and  $v_{out} = v_{in}$ . The capacitor charges to  $v_{in}$ .

- The output current  $I_{out}$  of the first amplifier will charge the capacitor.

$$\left. \frac{dv_C}{dt} \right|_{max} = \frac{1}{C} \frac{dQ}{dt} = \frac{I_{out}}{C}$$

- The bias current  $I_B$  of the second amplifier will drain the capacitor.

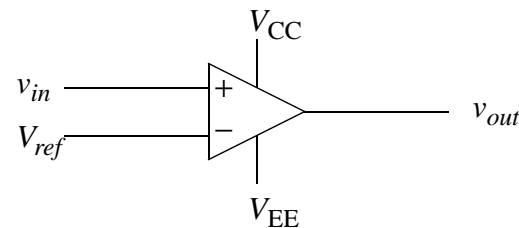
$$\left. \frac{dv_{out}}{dt} \right|_{droop} = \frac{I_B}{C}$$

- The control signal to the circuit  $v_{tr}$  is the *trigger*.

# Comparator

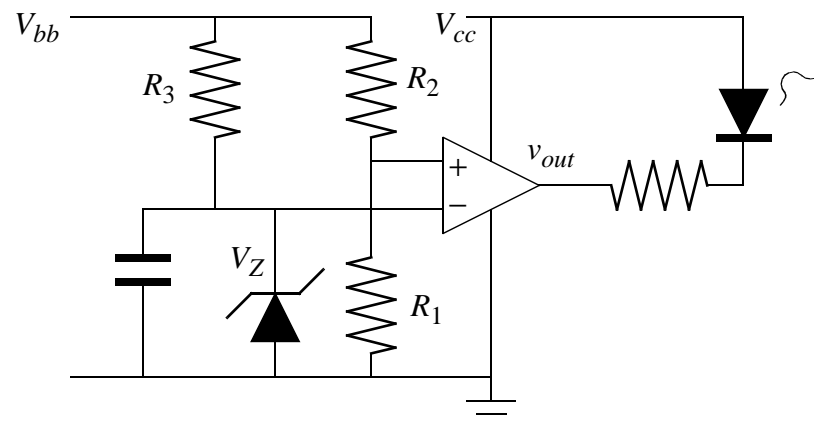
A comparator returns one of two values based on whether the input is greater or less than a reference value.

- Analog comparator



The logic states are  $v_{out} = V_{CC}$  if  $v_{in} > V_{ref}$ ;  $v_{out} = V_{EE}$  if  $v_{in} < V_{ref}$ .

- Low-battery indicator

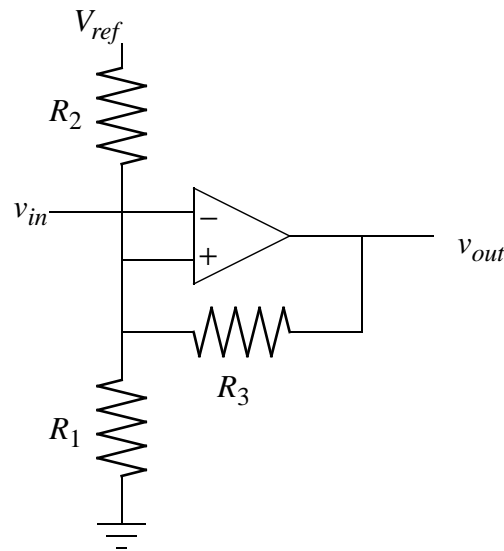


$V_{bb}$  is the value to be tested,  $V_{CC}$  supplies power to the tester.

# Schmitt Trigger

The Schmitt trigger is a circuit with binary output that has thresholds at two different voltages depending on the present state of the output.

- This combines analog elements with digital logic.
- Circuit diagram



The non-inverting input of the op-amp has a threshold which solely based on the three resistors and  $V_{ref}$  and  $v_{out}$ .

$$v_{th} = V_{ref} - i_2 R_2 = v_{out} - i_3 R_3 = i_1 R_1 = (i_2 + i_3) R_1$$

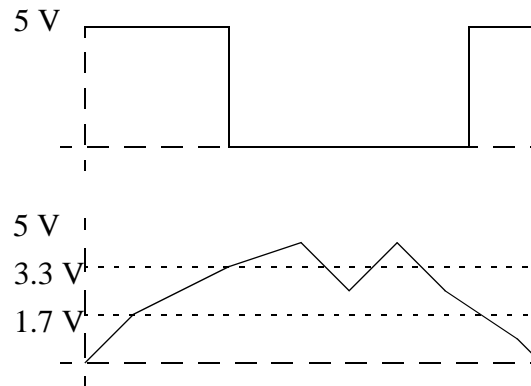
$$v_{th} \left( \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right) = \frac{V_{ref}}{R_2} + \frac{v_{out}}{R_3}$$

For equal resistors and 5 V supply,  $v_{th} = 1.67$  V or 3.33 V for  $v_{out} = 0$  V or 5 V respectively.

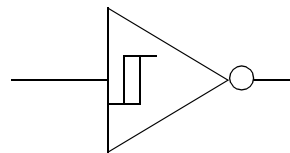
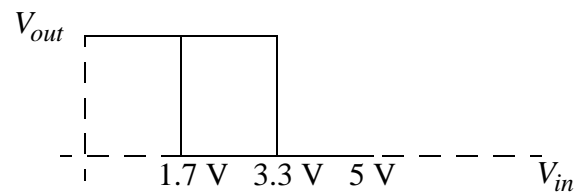
# Hysteresis

The circuit has one threshold when approaching from a low voltage state and a different one when approaching from a high voltage state. The effect of having different thresholds for different directions is called *hysteresis*.

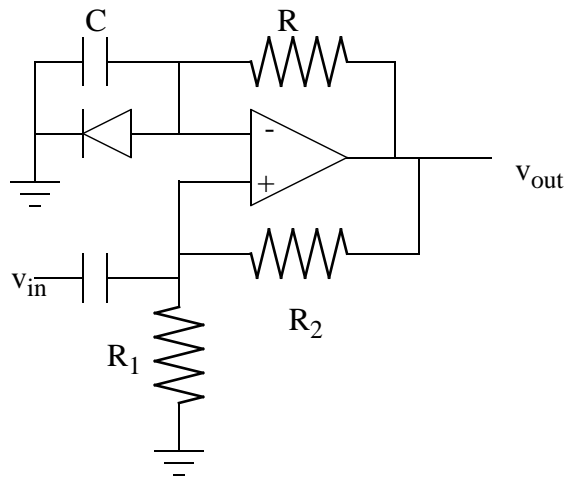
- Schmitt trigger timing



- Hysteresis curve



# Monostable



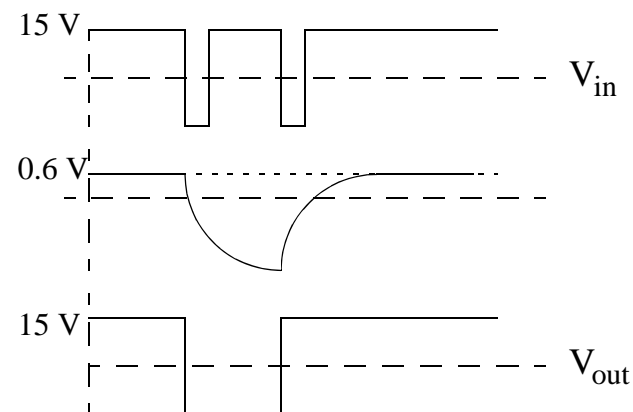
The monostable multivibrator (one-shot) is a device with two output states that has one stable state and another of fixed duration.

Here the negative feedback capacitor is shorted by a diode,  $V_C < 0.6$  V. When  $V_{out}$  is low the capacitor will discharge, but when  $V_{out}$  is high the capacitor will only charge to 0.6 V.

$$\frac{V_{out}R_1}{R_1 + R_2} = V_{out} + (V_D - V_{out})e^{-t/RC}$$

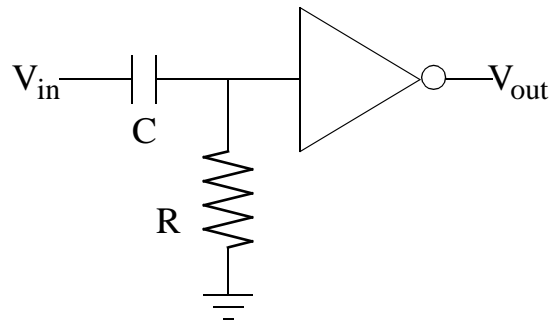
$$t = RC \log \left[ \frac{(V_{out} - V_D)(R_1 + R_2)}{V_{out}R_2} \right]$$

During the recovery (“dead time”) period as the capacitor is charging towards 0.6 V a new trigger would need to be sufficiently negative to permit refiring. With the resistor divider, this is not generally possible and no trigger is accepted during this period.

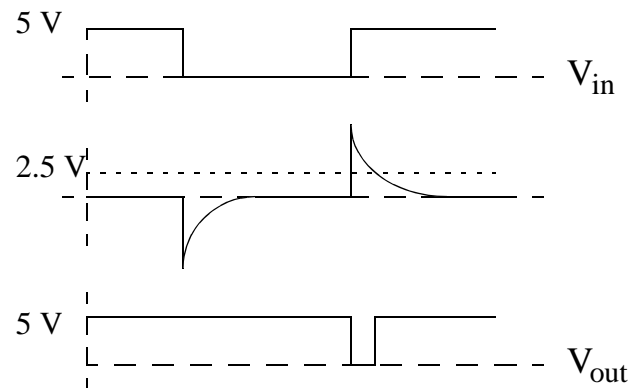


# Inverter One-Shot

- The input pulse is altered by the high-pass filter.



The falling edge of the input pulse has no effect, but the rising edge produces a pulse into the inverter that crosses the threshold for a time proportional to  $RC$ .

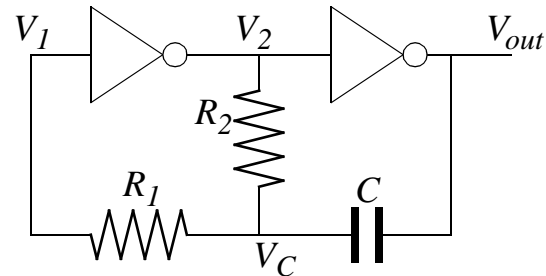


$$\frac{1}{2}V_0 = V_0 e^{-t/RC}$$

$$t = RC \log 2 = 0.693RC$$

# Astable Multivibrator

- Let the output of a monostable multivibrator feed back to retrigger another one-shot cycle.
- Double inverter oscillator



When  $V_{out} = +5$ ,  $V_C$  is charged towards ground from  $V_2$ .

As the input  $V_1$  drops below the logic threshold,  $V_2 = +5$  and  $V_{out} = 0$ .

When  $V_{out} = 0$ ,  $V_C$  is charged towards +5 from  $V_2$ .

The system oscillates between the two states.

$$R_1 \cong 10R_2$$

$$f \approx \frac{1}{R_2 C}$$

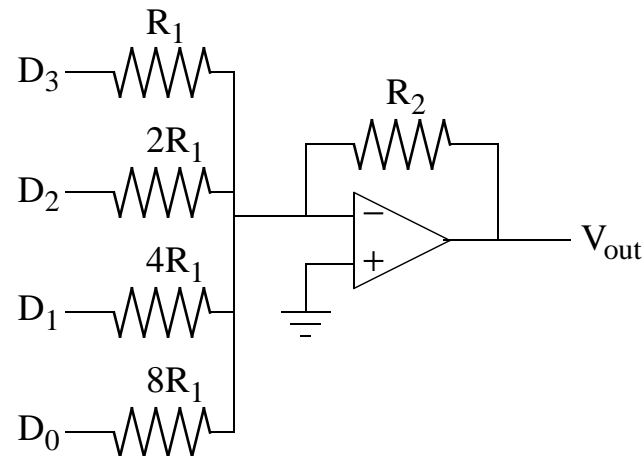
- This forms a clock that can oscillate at a defined frequency.

# Digital to Analog

## Op-Amp Summing Junction

The simplest DACs are derived from op-amps with different amplification ratios for different bits.

- Scaled Resistor Set



For  $D_n=0$  or 1, where 1 is set to  $V_{CC}$ , the output will be:

$$V_{out} = \frac{V_{CC}R_2}{R_1} \left( \frac{D_3}{1} + \frac{D_2}{2} + \frac{D_1}{4} + \frac{D_0}{8} \right)$$

For  $V_{CC}=5V$ ,  $R_2=1k\Omega$ , and  $R_1=1.25k\Omega$  the four individual resistors for the inputs would be 1.25k, 2.5k, 5k and 10k $\Omega$ . The nominal step between input values (LSB) is 0.5 V. The maximum  $V_{out} = 7.5 V$ .

# DAC Errors

- Dynamic range is insufficient.

For a large number of bits one needs a large range of resistors.

The amplifier must be able to drive the full range. For 16 bits this is a range of over 64000 from the lowest to highest possible value.

- Nonmonotonic behavior

For instance, let the 4-bit example above have input resistors with 10% tolerance. Within tolerance it is possible that these resistors are actually 1.37k, 2.25k, 4.5k and 9k. For a digital input of 7, the output voltage is  $5V * 1k\Omega / (1/2.25k\Omega + 1/4.5k\Omega + 1/9k\Omega) = 3.89 V$ . For a digital input of 8, the output voltage is  $5V * 1k\Omega / 1.37k\Omega = 3.65 V$ , an output lower than the one for 7.

- Nonlinear behavior

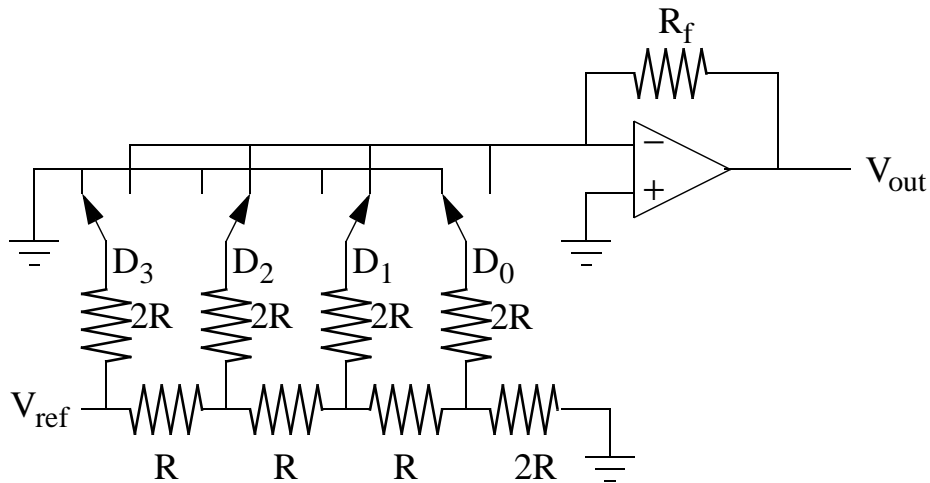
Similar to nonmonotonic errors, but the errors in the resistors are not large enough to cause one output value to be lower than the preceding one. An example from above would be to replace the 1.37k $\Omega$  resistor with a 1.25k $\Omega$  resistor. Inputs 6, 7 and 8 now give outputs of 3.33 V, 3.89 V and 4.00 V respectively. The steps of 0.56 V and 0.11 V are far from equal.

- Scale error

If in the 4-bit example the only error was that  $R_2 = 1.04 k\Omega$ . The steps would all be equal at 0.52 V. Full scale would be 7.8 V instead of 7.5V.

# *R-2R Ladder*

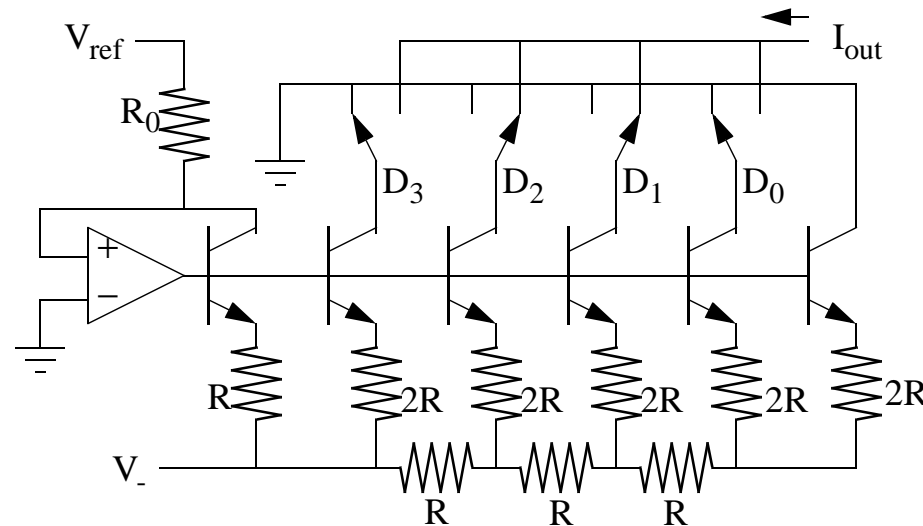
- Binary bits are converted to scaled currents.



- The equivalent resistance between V<sub>ref</sub> and ground is R, regardless of the switches, since the op-amp will hold the non-inverting input to ground as well.
- Half the current from V<sub>ref</sub> goes towards D<sub>3</sub>, 1/4 goes towards D<sub>2</sub>, 1/8 goes towards D<sub>1</sub>, and 1/16 goes towards D<sub>0</sub>. The op-amp sums the input currents and multiplies them times R<sub>f</sub> to get V<sub>out</sub>.
- An analog switch would be needed to convert binary signals into switch controls.
- Note that only two resistor values are needed.

# Current Switch IC

- These chips use the R-2R ladder design directly with transistors to make an analog current proportional to the binary number input.

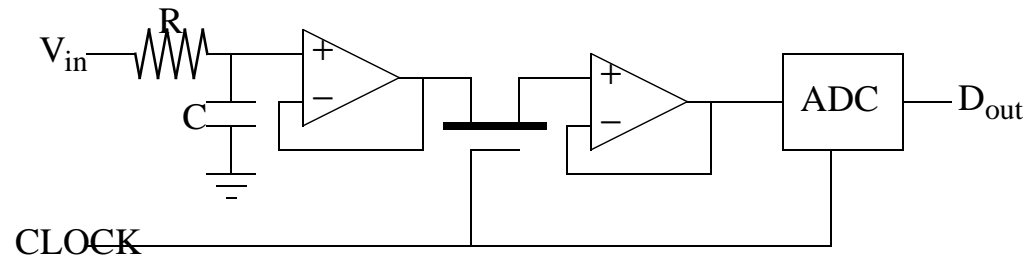


The op-amp will hold the non-inverting input to ground drawing a current from  $I_{ref} = V_{ref}/R_0$ . That current flows into the collector of the transistor and the op-amp will hold the base such that  $I_C = I_{ref}$ . That means that  $V_E - V_- = I_{ref}R$ .

- The voltage at all the emitters will be the same and the R-2R ladder will again cause each transistor in line to draw half the current of the preceding one.

# Analog to Digital

A simple model of analog to digital converter requires a smooth signal, sampled before digitization.



The above circuit shows the three basic parts:

1. Low pass filter
  2. Sample-and-hold circuit
  3. Digitizer
- The clock controls the sampling speed of the ADC.

# Sampling Errors

Once a clock establishes a sampling time  $T$  there are errors that can occur in the digitization. The two possibilities are:

1. The sampling time is too slow.

The changes in analog values will be missed in the digital values. Ideally every change in the input signal that is at the level of the LSB should be captured by the digital output. For slowly changing signals maximum slope ( $s$  in V/s) sets the needed sampling time.

$$T < \frac{V_{LSB}}{s}$$

2. The sampling time is too fast.

If the sampling time is fast compared to noise on the input signal, and the noise is of a magnitude greater than the LSB it will be preserved and possibly enhanced by the digitization process. To avoid sensitivity to noise (with frequency  $f_N$ ), it needs to be filtered, or set the sampling time to a larger value.

$$T > \frac{1}{f_N}$$

# Nyquist Sampling

- Nyquist theorem:

For proper sampling  $\omega_{\max} < \pi/T$  (or  $T < 1/2f_{\max}$ ).

So, if the minimum time for a signal to change is  $t_{\min}$ , the sampling time must be less than half.

- There is still the problem of high frequency noise.

The noise will be picked up in the frequency spectrum as the noise frequency is shifted by  $2\pi n/T$  by the sampling process.

The solution is to filter all frequencies above  $1/2T$  to insure the Nyquist condition is met.

Use  $RC=T$  in a low pass filter.

- The sampled digital signal  $d(t)$  of a real signal  $v(t)$  can be expressed as the sum of discrete values at

the time of the sample. 
$$d(t) = \sum_{n=-\infty}^{\infty} v(t)\beta\delta(t-nT) = v(t) \sum_{n=-\infty}^{\infty} \frac{\beta}{T} e^{2\pi jnt/T}$$

- The Fourier transform of the sampled signal,  $h(\omega)$ , is:

$$h(\omega) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{\infty} v(t) \left( \sum_{n=-\infty}^{\infty} \frac{\beta}{T} e^{2\pi jnt/T} \right) e^{-j\omega t} dt = \frac{\beta}{T} \sum_{n=-\infty}^{\infty} g\left(\omega - \frac{2\pi n}{T}\right), \text{ where } g(\omega) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{\infty} v(t) e^{-j\omega t} dt.$$

- The initial analog signal is preserved in the digital sample, but repeated with a shift every  $2\pi/T$ . If there is no overlap in the repeating  $g(\omega)$ , then a filter can select just that part of the frequency spectrum. This is true if  $\omega_{\max} < \pi/T$ .

# Flash ADC

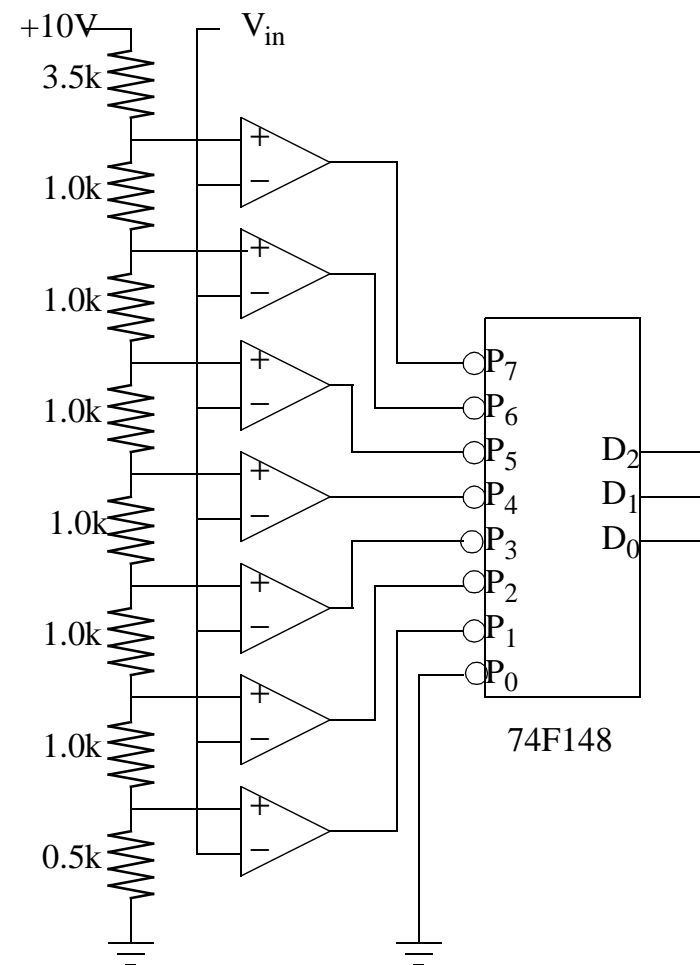
- The parallel encoder is an example of a *flash* ADC.

The name comes from the very fast conversion from analog to digital.

- The 3-bit example shown has no clock and converts as soon as the  $V_{in}$  changes, limited by the speed of the comparators and priority encoder (74F148).

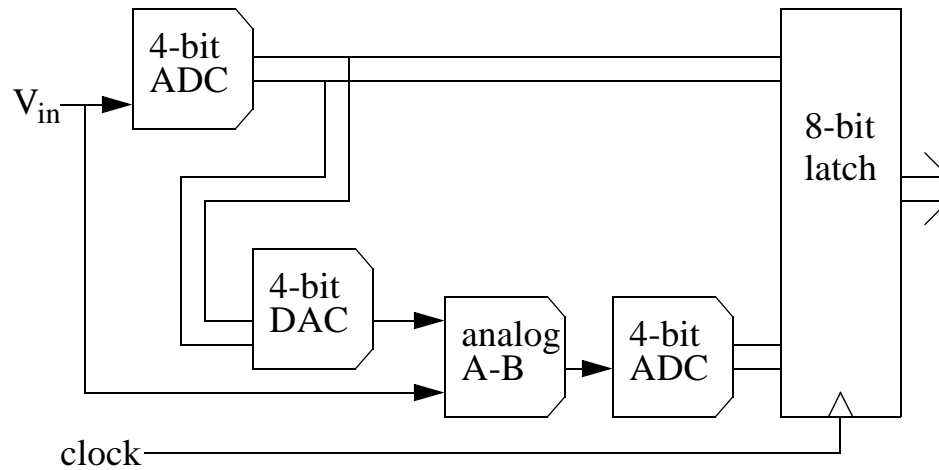
- In general a flash ADC would have a clock controlling an output enable to a latch, so that the digital values would only change at set times.

- Flash ADCs require one comparator for each value. An 8-bit ADC would require 256 separate comparators with separate voltage settings.



# Half-flash ADC

- At the cost of some speed a *half-flash* ADC can be constructed from two smaller flash ADCs.

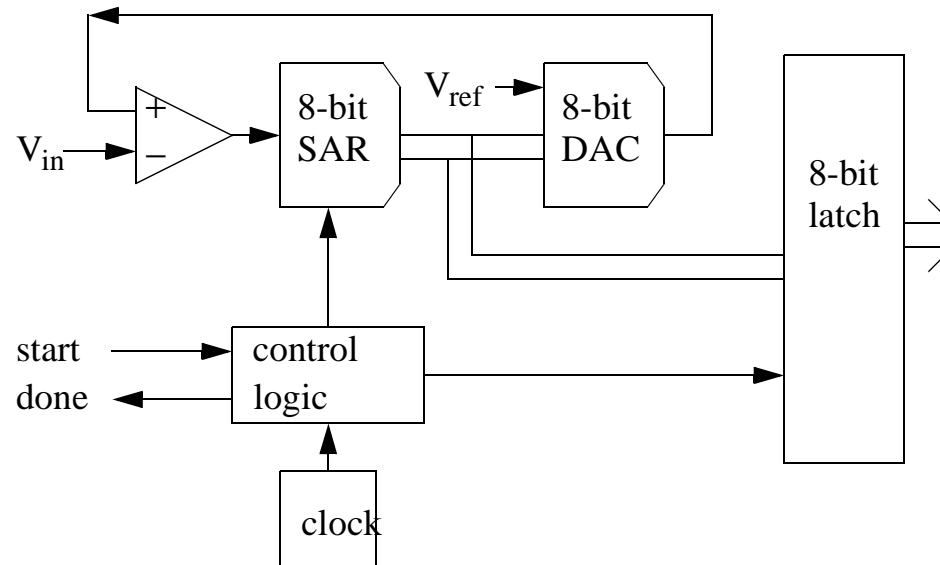


- The input voltage is digitized by a coarse ADC filling bits 4-7.
- The output is converted back to an analog value.
- The converted value is subtracted from the original voltage forming an analog remainder.
- The remainder is digitized by a fine ADC filling bits 0-3.
- An external clock controls the latch insuring all steps are completed before the output is updated.

# Successive Approx.

The basic units of a successive approximation ADC are:

1. Comparator - Compares the input analog value to the current approximation.
2. Successive Approximation Register (SAR) - The SAR starts with 1 in the MSB and 0 for all other bits. With each clock input the SAR resets the current bit if the comparator is HIGH and moves to the next bit down by setting it.
3. DAC - Converts the bit pattern from the SAR into an analog value for the comparator.
4. Latch - Stores the bit pattern when the LSB is complete.
5. Control Logic - Counts  $n$  clock pulses to the SAR then sends DONE to the latch.



### Successive Approximation ADC Example

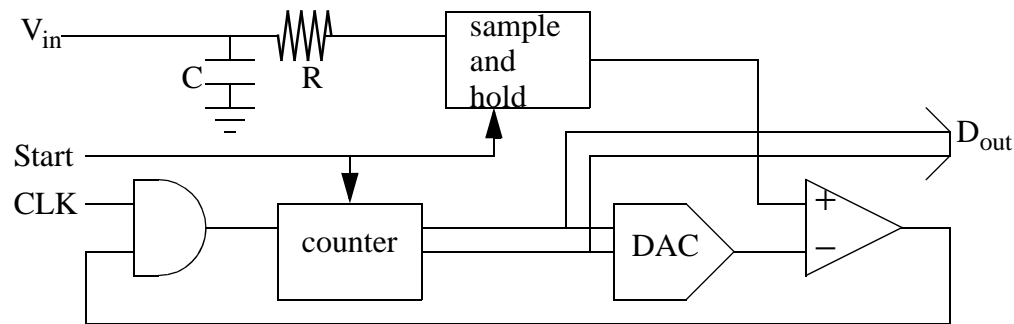
For an 8 bit ADC set  $V_{ref}$  to 5.12 V so the LSB is set to 20 mV.

Clock	SAR	DAC
START	10000000	2.56 V
CLK 1	11000000	3.84 V
CLK 2	10100000	3.20 V
CLK 3	10010000	2.88 V
CLK 4	10011000	3.04 V
CLK 5	10010100	2.96 V
CLK 6	10010110	3.00 V
CLK 7	10010111	3.02 V
DONE	10010110	3.00 V

The process takes 8 clock cycles to get a result. For a 1 MHz clock this would result in a digitization time of 8  $\mu$ s. This would require a DAC that could convert in less than 1  $\mu$ s.

# Counter ADC

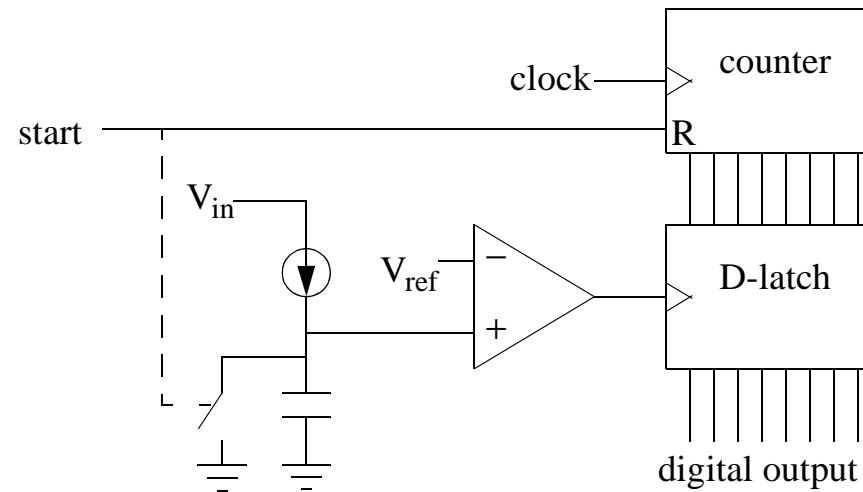
- A simple circuit that uses a clock, a counter, a DAC and a comparator to match to an input analog signal.
  1. An external start signal resets the counter and operates the sample-and-hold circuit.
  2. The output of the counter is converted into an analog value by a DAC.
  3. When the DAC output matches the input voltage, the clock is stopped and the digital value is read out.



- The circuit is only as fast as the time it takes for the counter to reach full scale:  $2^n T_c$ .
- The output will be as precise as the DAC that is used by the comparator.
- The DAC must be faster than the clock.

# *Integrating ADC*

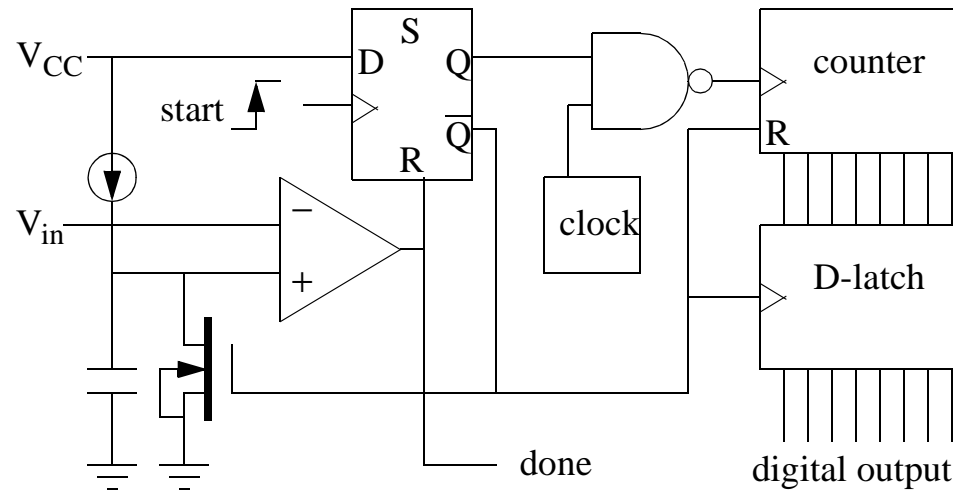
1. Convert a voltage into a current.
2. Use the current to charge a capacitor yielding a time proportional to the input voltage.
3. Measure the time with a digital counter operated at a fixed clock frequency.



- The time can be measured as the capacitor charges, discharges or both.

# Single Slope

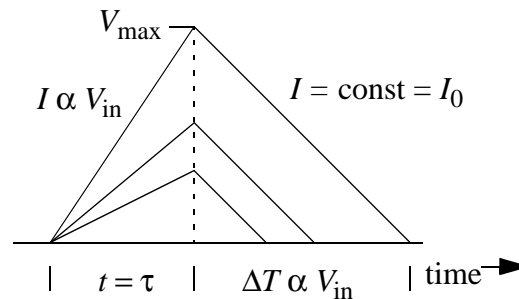
- Single slope integration relies on the stability of the capacitor and comparator to get an accurate reading.



1. A start pulse clocks a D-flip-flop causing it to go HIGH and allowing the clock to increment a counter.
2. The  $\bar{Q}$  output of the flip-flop turns off an FET and the capacitor begins a linear ramp for  $t = CV/I$ .
3. At that time the comparator goes HIGH and resets the flip-flop, latching the counter output and signalling the end of the digitization.
4. The reset also clears the counter and discharges the capacitor through the FET.

# Dual Slope

- One solution to the strict requirements on a single slope-integrator is to use the capacitor for both the reference and signal integration so that the effects of the capacitor cancel on the two measurements. This is called *charge-balancing*.
- Charge balancing also eliminates external noise by integrating over a longer time and letting any noise be averaged out.



- Dual slope integration charges the capacitor for a fixed time from a current source set by the input voltage;  $V_{\max} = I_{\text{in}}\tau/C$ .
- The same capacitor is discharged with a constant current sink that is measured with a counter;  $\Delta T = V_{\max}C/I_0$ .
- The measured time is then  $\Delta T = I_{\text{in}}\tau/I_0$ .
- If the same clock is used for both slopes, it also is cancelled out.